OZ960 Design Reference

Intelligent Lighting Group

Scope

This Application Note covers the functions and features of the OZ960 inverter controller through a functional description of each pin. In addition, it discusses the full-bridge inverter topology, transformer design and selection, selection of LPWM dimming control components, PCB layout and reference design notes for a typical application circuit suitable for Cold Cathode Fluorescent Lamp (CCFL) backlight applications.

Introduction

CCFL's are utilized in LCD displays which include notebook, monitor, television, DVD and GPS applications. A CCFL requires a high AC voltage (typically 600Vrms) for normal operation and requires a current between 2mArms to 6mArms. Prior to normal operation, a CCFL typically requires a much higher AC voltage (typically 1500Vrms) to ignite and induce current flow. The lamp current and voltage waveforms must be as sinusoidal as possible to reduce EMI/RFI emissions. Good sinusoidal waveforms result in good electrical to light conversion efficiency.

In most applications, the power supply provides a DC voltage and a high-efficiency DC-AC inverter is required to drive the CCFL. The inverter must also provide a scheme for dimming control to adjust the panel brightness.

The OZ960 is a unique, high-efficiency, CCFL backlight inverter controller that is designed for wide input voltage inverter applications. It performs the CCFL dimming control function with an analog voltage or a Low-frequency Pulse Width Modulation (LPWM).

Operating in a zero-voltage switching, full-bridge configuration, the inverter circuit achieves a very high power conversion efficiency. In addition, the transformer used with the OZ960 does not require any specific gap-less arrangement. It provides designers a high degree of design flexibility in selecting transformers. The IC provides a symmetrical square-wave voltage drive to the transformer. The transformer leakage inductance and the output capacitance, connected in parallel with the transformer secondary winding, form a resonant tank. The single-stage topology, shown in Figure 1, page 2 converts a DC voltage to an AC voltage and amplifies this voltage which produces a sinusoidal waveform. The single-stage resonant tank converts the square-wave voltage to a sinusoidal output to drive the CCFL. The sinusoidal CCFL voltage and current waveforms produce minimal harmonic EMI/RFI emissions. This also results in good electrical to light conversion efficiency. The transformer does not require an expensive center-tapped primary, avoiding a less reliable secondary fold-back treatment.

The OZ960 functions in a constant PWM mode operation. Depending on the CCFL and transformer characteristics, the typical normal operating frequency is in the range of 30kHz to 85kHz. The built-in LPWM dimming control provides a wide dimming range that simplifies the application circuit design. The operating frequency and the LPWM frequency are both user-programmable.

BLOCK DIAGRAM OF SINGLE-STAGE INVERTER USING OZ960

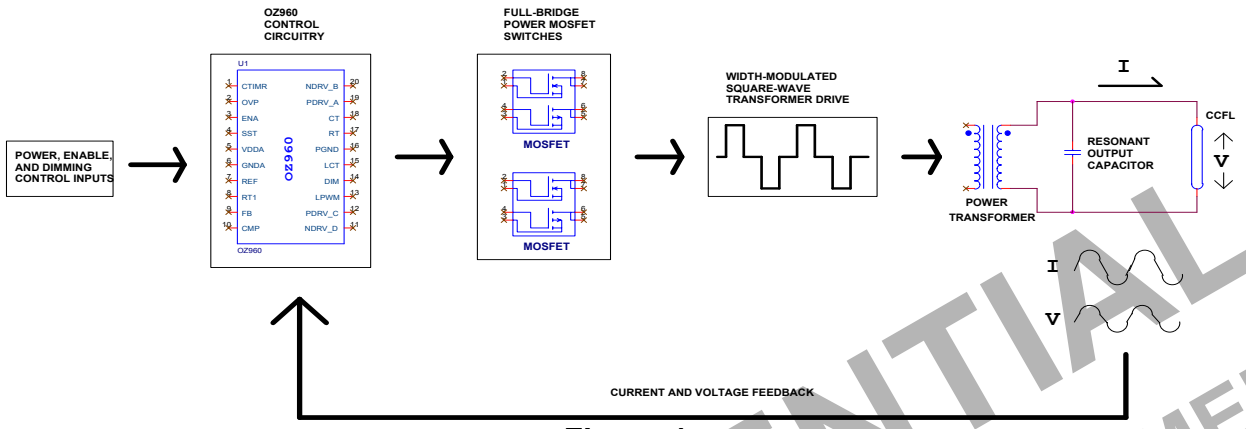


Figure 1

OZ960 Inverter Controller Pin-By-Pin Functional Description

The OZ960 is available in a 20-pin plastic SSOP, SOP and DIP package. The functional block diagram of the IC is shown below. A detailed description of each pin is provided in the next section.

OZ960 FUNCTIONAL BLOCK DIAGRAM

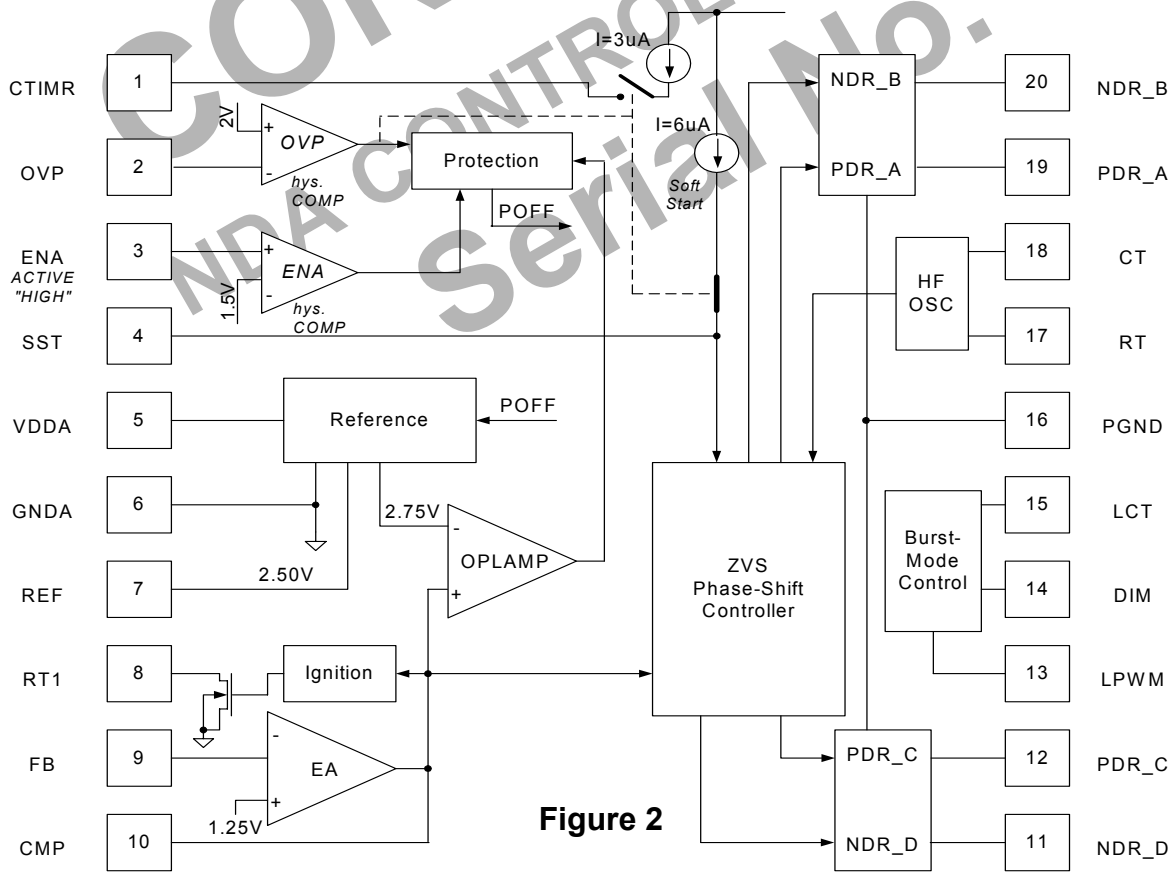


Figure 2

OZ960 Pin Description (Refer to Figure 2, page 2 and Figure 5, page 13)

Pin 1: CTIMR - Ignition timing capacitor pin. CTIMR provides the timing control for CCFL ignition by connecting an external capacitor C9 to ground. The ignition time varies with CCFL length, diameter, module packaging and temperature. An external capacitor C9 is selected to determine the necessary striking time. When OVP (refer to pin 2) reaches the 2.0V threshold, the capacitor begins to charge with a 3uA current. When CTIMR voltage reaches 3.0V, the IC will immediately shut down (latches). An off/on cycle of the OZ960 power supply is required to reset the latch. The capacitance value of C_{CTIMR} (C9) is selected to provide enough time Δt for the CCFL to ignite (approximately 1 second). The relation is given by the following equation:

$$C_{CTIMR}(\mu F) = \Delta t(s)$$

Pin 2: OVP – Over-Voltage Protection pin. This input pin receives a voltage feedback from the CCFL output voltage. The signal is used by the OZ960 to regulate the output voltage during striking or open-lamp condition through a voltage feedback loop. While striking or in an open-lamp condition, the SST (Soft Start Time, pin 4) voltage controls the gradual increase of the output voltage through a charging capacitor C12. The feedback voltage is obtained by adding a capacitor C10 in series with the output resonant capacitor C4 to form a capacitive voltage divider. Capacitor C10 has much lower impedance than the main output capacitor C4, so that the effect on the resonant characteristics is negligible. The voltage on capacitor C10 is peak-detected through a RC circuit. The OVP voltage is compared to a 2.0V threshold by the internal comparator. Once the 2.0V threshold is reached, during striking or open-lamp condition, the IC clamps the SST voltage to its current level. Thus, the output voltage is maintained at the level set by the voltage divider. At this moment, CTIMR capacitor C9 begins to charge and the IC will shut down when it reaches 3.0V.

Pin 3: ENA - Enable pin. Enables operation of the IC. Apply >2.0V to enable, <1.0V to disable.

Pin 4: SST - Soft-Start Time pin. Connecting an external capacitor C12 from this pin to ground provides the soft-start function. A charging current of 6uA is provided to capacitor C12. At start-up, as C12 charges to Vcc, the voltage level controls the gradual increase in the power MOSFET drive overlap; which determines the output current/voltage. This reduces in-rush current and avoids unnecessary stresses with the other inverter components and the CCFL lamp. This pin also enables the open-lamp protection function when it reaches a threshold of approximately 1V below the VDDA (power supply, pin 5) voltage. For a nominal VDDA of 5.0V, the threshold is 4.0V.

Pin 5: VDDA - Power supply for OZ960, +5V nominal.

Pin 6: GNDA - Signal ground pin. All low-current signals must be grounded to GNDA. The high-current signals such as the transformer and MOSFET grounds must be connected to the power ground PGND (pin 16). GNDA and PGND are connected at the input connector ground.

Pin 7: REF - Reference voltage pin. This is the 2.5V output of the internal regulator, which provides biasing to the internal circuitry. This pin can source a maximum current of 1mA.

Pin 8: RT1 - Striking frequency pin. A higher oscillator frequency is usually required by the inverter to provide a sufficient striking voltage. This pin provides an option to raise the frequency during striking. An external resistor R9 is connected in parallel from this pin to RT (pin 17). An external resistor R4 from RT to ground and an external capacitor C8 from CT (pin 18) to ground sets the normal operating frequency. During striking, RT1 is connected internally to signal ground. During striking, RT1 resistor R9 is in parallel with RT resistor R4. Thus, the resistance from RT to ground is reduced. This increases the oscillator frequency. After the CCFL ignites, RT1 is open (high impedance) and the striking frequency switches to a lower normal operating frequency. CMP (pin 10) controls the switching of RT1. During striking, CMP is high and switches RT1 ON. After ignition, CMP goes low and switches RT1 OFF.

Pin 9: FB - Current-sense feedback pin. This is the inverting input to the internal error amplifier. The FB pin accepts an averaged half wave sinusoidal voltage. The half wave voltage is derived from the lamp current detected by a sense resistor R13. The FB voltage is compared to an internal reference voltage of 1.25V nominal (non-inverting input to the error amplifier). The output of the internal error amplifier (CMP) controls the power MOSFET drive overlap such that FB is maintained at 1.25V. Thus, the lamp current I_{lamp} is regulated and is related to the sense resistor (R_{sense}) by the following equation.

$$I_{lamp} = 1.25/(0.45 \text{ X } R_{sense}) = 2.78/R_{sense}$$

Using the above equation, a CCFL requiring a current of 5mA requires a R_{sense} resistor value of 556Ω.

$$R_{sense} = 2.78/5 = 556\Omega$$

Pin 10: CMP - Compensation pin. This is the output of the internal error amplifier. An external capacitor C16 is connected from this pin to FB for feedback loop compensation. CMP controls the power MOSFET drive overlap to regulate the CCFL current. During striking, no CCFL current is detected, therefore the FB voltage is low and CMP voltage is high (>3V). When the CCFL ignites, the FB voltage rises and the CMP voltage drops to the normal operating level. During normal operation, CMP also provides the trigger signal for the open-lamp protection function. If the CCFL is suddenly removed or damaged (open) during operation, CCFL current is no longer sensed and the FB voltage drops. This causes the CMP voltage to rise. When the CMP voltage reaches the 2.75V threshold, the OZ960 shuts down (latches). A power off/on cycle is required to reset this latch.

Pin 11: NDR_D - One of two N-MOSFET gate drive outputs. The duty cycle is fixed at 50%.

Pin 12: PDR_C - One of two P-MOSFET gate drive outputs. PDR_C switches high and low with NDR_D. There is a 380ns break-before-make period between NDR_D and PDR_C transitions that prevents simultaneous conduction of the N and P MOSFETs.

Pin 13: LPWM – LPWM dimming signal pin. This is the low-frequency PWM output for PWM dimming operation. The typical range is 150Hz to 400Hz. This pin outputs periodic pulses of 2.5V peak alternating with a high-impedance state. The frequency is determined by the LCT (pin 15) capacitor C13 value. A resistor value R11 is connected from this pin to the FB pin. FB is then periodically switched slightly higher than the 1.25V reference (internal non-inverting input of the error amplifier). This results in CMP being periodically switched low and high. If CMP is high, the inverter outputs full lamp current. When CMP is low, the inverter outputs no current. The duty cycle of this switching varies the average lamp current and thus the panel brightness. A DC voltage input to the DIM pin (pin 14) determines the duty cycle.

Pin 14: DIM - Dimming voltage pin. This is the input pin for LPWM dimming control. The voltage on this pin is compared to the LCT (pin 15) triangular waveform to produce a pulse-width modulated (PWM) output. The DIM pin accepts an analog voltage range of 1.0-3.0V to provide a LPWM duty cycle of 0-100%.

Pin 15: LCT - PWM timing capacitor pin. A capacitor C_{LCT} (C13) for LPWM dimming is connected from this pin to ground. The voltage at this pin is a triangular waveform with peak of 3.0V and valley of 1.0V. The LPWM frequency f_{burst} is set by the following equation.

$$f_{burst}(Hz) = 1496/C_{LCT}(nF)$$

Pin 16: PGND - Power ground pin. All high-current signals must be grounded at this point. These are the source pins of the N-MOSFETs, supply capacitor C1 ground, transformer ground, current sense resistor R13 ground and the voltage sense capacitor C10 ground. It is recommended to have a ground plane (wide-area copper trace) for PGND in the PCB layout.

Pin 17: RT - Main oscillator timing resistor pin. Together with the CT (pin 18) capacitor C8, a resistor R4 from this pin to ground determines the switching frequency.

Pin 18: CT - Main oscillator timing capacitor pin. Together with RT, a capacitor C8 to ground sets the switching frequency of the four output drives, PDR_A, NDR_B, PDR_C and NDR_D. CT is a triangular waveform with a peak of 3.0V and a valley of 1.0V. The switching frequency is calculated by the following equation.

$$f_{SW}(kHz) = 68.5(10^4)/[RT(k\Omega) \text{ X } CT(pF)].$$

Pin 19: PDR_A - The second P-MOSFET gate drive output. Similar to PDR_C, this switches simultaneously with NDR_B with a break-before-make period of 380ns.

Pin 20: NDR_B - The second N-MOSFET gate drive output. The duty cycle is fixed at 50%.

OZ960 Full-Bridge Inverter Topology

Referring to Figure 5, page 13, the OZ960 drives a full-bridge power train where the transformer couples the energy from the power source to the secondary CCFL load. The full-bridge switch is configured such that U1 N-MOS and U3 P-MOS are ON while U1 P-MOS and U3 N-MOS are OFF in a half-cycle. During the next half cycle, U1 N-MOS and U3 P-MOS are OFF while U1 P-MOS and U3 N-MOS are ON. This develops an alternating current through the transformer primary. The ON duration of the switches determines the amount of energy delivered to the CCFL. The ON duration of each switch pair is equal.

The CCFL current is sensed via resistor R13 and regulated through the adjustment of the ON-time for both switch pairs. This is accomplished through an error amplifier in the current feedback loop. A soft-start circuit ensures a gradual increase in the input and output power which significantly increases CCFL lamp life and reduces stress on the other external components. The soft-start capacitor determines the rise rate of the voltage on the SST pin, where the voltage level determines the ON-time of the switch pairs. This minimizes high current surges in the circuit.

Applying an enable signal to the ENA pin of the IC after the bias voltage is applied to VDDA, initiates the circuit operation. The output drives PDR_A, NDR_B, PDR_C, and NDR_D generate complementary square pulses. The pulse frequency is determined by R4 and C8, when connected to the RT and CT pins respectively. Initially, the energy converted from the power source to the CCFL is low due to the soft-start function. The energy increases as the soft-start capacitor voltage increases linearly with time. The voltage at the secondary side of the transformer T1 increases correspondingly. This process continues until the lamp ignites, CCFL current is detected through R13 and is regulated. The detected CCFL current is converted to a voltage fed into the FB pin – inverting input to the internal error amplifier. The output of the error amplifier, CMP, varies to maintain the FB voltage at the 1.25V level. The CMP level controls the ON-duration of the MOSFET switch pairs. As a result, the CCFL current is regulated at a level determined by the value of R13. The operation of the four switches is implemented with zero-voltage switching to achieve high-efficiency power conversion.

Design Procedure for OZ960 Inverter

A CCFL inverter design involves the consideration of important factors such as input voltage, lamp current/voltage, leakage capacitance of the LCD panel and transformer parameters. The entire design procedure can be greatly simplified by starting with a reference design. Referring to Figure 5, page 13 you will find an OZ960 application circuit suitable for the following application:

Input voltage: 9V - 21V
Lamp current: 6.0mA
Lamp voltage: 650V
Output power: 3.9W

Operating frequency: 61kHz +/- 8%
Striking frequency: 75kHz +/- 8%
Striking voltage: 1400Vrms minimum
Striking time: 1 second
Typical efficiency: 87%

The following sections illustrate the basic design procedure for an OZ960 inverter wherein the transformer design, operating frequency setting, dimming control method, striking voltage control, open-lamp protection and frequency compensation for the control loop are highlighted. Also provided are design tips on the PCB layout, as well as, design notes and a reference application schematic.

Transformer Design for OZ960 Inverter

The most complicated component in an inverter design is the output transformer. A critical parameter of the transformer is the leakage inductance. OZ960 utilizes the leakage inductance associated with a parallel and/or series capacitor to generate a sinusoidal drive for the CCFL. For a 13" or 14" LCD panel used in a notebook computer, a typical leakage inductance of 150mH is applicable. The following is a list of parameters for a typical transformer used in a notebook application:

Primary inductance: 90μH
Secondary inductance: 380mH
Leakage inductance: 150mH
Turns ratio: 78 (28:2200)
Power rating: 4.0w
Voltage rating: 1500Vrms

Normally, the coupling between the windings of a high-voltage transformer is loose such that the associated leakage inductance is high. Transformer makers can adjust the leakage inductance by gapping the core or arranging the coupling between windings. For other applications, the inverter designer should adjust the parameters according to the system specification. A detailed discussion is included in the following section.

Steps in the Selection/Design of Transformer and Output Stage Components

1. Determine the core to be used. Make sure that the power rating is sufficient for the intended application. Most transformer vendors provide power ratings.
2. Choose the number of primary turns such that it will not saturate the core. The following relation which is derived from Faraday's Law:

$$N_P = V_{IN} \times t_{ON}/(\Delta B \times A_e)$$

N_P = Minimum number of primary turns
V_{IN} = Input voltage (V)
t_{ON} = ON-time of the N-MOS, duty cycle (overlap of diagonal switches) times half the period (μs)
ΔB = Core flux density swing (T)
A_e = Smallest cross-sectional area of the core where flux flows (mm^2)

A transformer used in a full-bridge topology operates in two quadrants of the B-H curve so that the maximum flux density B_{max} = ½ ΔB. For most cores, the acceptable maximum flux density to prevent saturation is 200mT. An example with a nominal input voltage of 15V, operating frequency of 61kHz, duty cycle of 55% and core cross-sectional area of 8 mm^2, the minimum number of primary turns required is 21. For our reference design, 28 turns is sufficient which provides a flux density of 149mT.

3. Determine the required secondary turns to meet the required secondary RMS voltage. Referring to the reference design (Figure 5), the required secondary RMS voltage (CCFL voltage) is 650V, minimum input voltage is 9V and the number of primary turns is 28. Therefore, for the secondary turns, we need at least 650/9 X 28 = 2022 turns. The reference design uses 2200 turns which is typical for most applications.

4. Select the proper wire gauge of the windings so that no excessive heating is generated, especially in the primary winding, which carries a higher current. Normally, for transformers used in inverter applications, it is desirable to have a temperature rise of less than 30°C.

5. Determine the value of the output resonant capacitor C4. Designer selects the operating frequency first based on the LCD panel specifications. Once the operating frequency is decided, the inductance, leakage inductance of the transformer and the output capacitor can be determined. There are two resonant frequencies to consider in choosing this capacitor: 1) the resonant frequency of the output capacitor with the main inductance of the transformer secondary and 2) the resonant frequency of the output capacitor with the leakage inductance of the transformer secondary. The selected operating frequency is between these two resonant frequencies.

   As an example, for a typical 13" or 14" LCD monitor design, the secondary inductance of the transformer (28:2200 turns ratio) is approximately 380mH and the leakage inductance is approximately 150mH.

   To determine the required output capacitance for C4, assume that designer selects the inverter operating frequency of 60KHz. Also, assume that the LCD panel possesses 10pf parasitic capacitance that is effectively in parallel with output capacitor. Based one the transformer parameters above, the output capacitor of 18pf yields 50KHz and 78KHz for the two resonant frequencies respectively.

The operating frequency is set by selecting RT and CT component values to satisfy the following equation:

$$f_{operating} = \frac{68.5\ (10^4)}{RT(k\Omega)\ CT(pF)}$$

6. Additional fine-tuning may be required for good symmetrical CCFL current and voltage waveforms and/or to provide a good margin for a minimum startup voltage. This can be done by adjusting the operating frequency around the value obtained above and/or adjusting the turns ratio of the transformer.

Selection of Dimming Control Components

The OZ960 provides internal LPWM dimming control circuitry for wide dimming range applications. The input to this circuit is an analog voltage of 1.0-3.0V applied to the DIM pin which produces a LPWM duty cycle of 0-100%. A resistive network (R3, R5 and R8) is usually inserted between the external dimming input and the DIM pin (refer to Figure 5, page 14) to enable different external dimming input ranges (typically 0.0-3.0V, 0.0-3.3V or 0.0-4.0V).

The output of the internal LPWM circuit, LPWM voltage, is a low-frequency PWM signal with a peak ON level of 2.5V and a high impedance OFF state. Resistor R11 from the LPWM pin to the FB pin completes the external PWM circuitry. The resistor value must be chosen such that FB (error amplifier inverting input) can be periodically pulled higher than the internal 1.25V threshold (error amplifier non-inverting input). This results in the error amplifier output CMP being periodically switched low and high. Consequently, the lamp current output is alternately turned off/on, accomplishing LPWM dimming.

Figure 3, page 9 illustrates the dimming operation.

BURST-MODE (PWM) DIMMING CONTROL

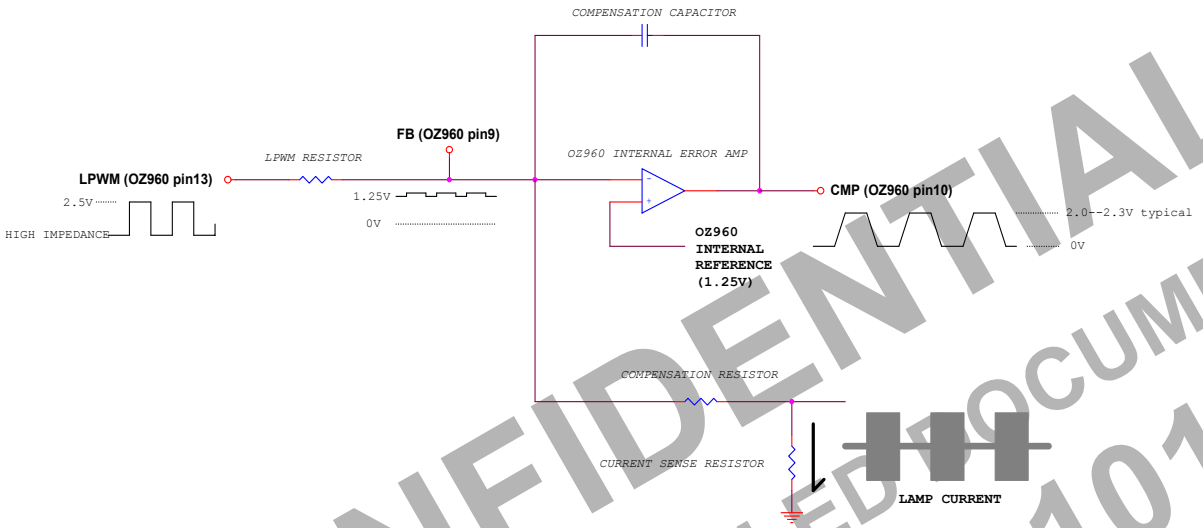


Figure 3

The frequency f_{burst} of the LPWM control can be set externally through capacitor C_{LCT} (C13) at the LCT pin to ground and can calculated by the following equation:

$$f_{burst}(Hz) = 1496/C_{LCT}(nF)$$

Striking Frequency Control

Usually, it is necessary to increase the switching frequency during the striking period to obtain a high striking voltage level. The OZ960 provides the RT1 pin for this purpose. Resistor R9 is connected from this pin to the RT pin. The RT1 pin is connected to ground during the striking period (approximately 1 second on start-up), that is, the RT1 resistor R9 is in parallel with the RT resistor R4. Thus, the effect is a higher frequency. The striking frequency must be set near the resonant frequency of the output capacitor C4 and the secondary leakage inductance. This higher frequency produces a high enough RMS voltage to ignite a CCFL. The RT1 resistor provides the flexibility to set a range of striking voltages needed for a variety of CCFL specifications. After ignition, RT1 is disconnected from RT, which dictates the lower normal operating frequency, which is determined by RT and CT.

Striking Voltage Control/Overvoltage Protection

The OZ960 protects the inverter and the transformer from excessive output voltage. This is accomplished through the OVP pin. An external capacitor C10 is added in series to the output resonant capacitor C4 to form a capacitive voltage divider (refer to Figure 5, page 13). The capacitance value of C10 is much higher than the main output capacitance value of C4. The typical value of C10 is between 15nF and 33nF compared to the 18pF value of C4, which has a negligible effect on the resonant characteristics.

Capacitor C10 is chosen such that it provides a peak voltage of ~2.0V at the desired RMS striking voltage. The RMS striking voltage is approximately equal to the ratio of the lower divider capacitor C_L (C10) to the upper divider capacitor C_U (C4) by using the following equation:

$$V_{striking}\ (Vrms) = C_L\ (pF)/C_U\ (pF)$$

For example, if C_L = 33nF = 33,000pF and C_U = 22pF, then the RMS striking voltage is $V_{striking}$ = 33000/22 = 1500Vrms. The peak voltage is detected through a parallel RC circuit and inputted to the OVP pin, which is the input to an internal comparator, with a 2.0V reference. If the 2.0V threshold is reached, the comparator clamps the output duty cycle (overlap conduction of diagonal switches in the full-bridge topology) to achieve a constant RMS voltage determined by the capacitive voltage divider.

Striking Time Control

The OZ960 provides flexibility in setting the striking time for a CCFL. The capacitive voltage divider (C4 and C10) is set such that when the output reaches the maximum striking voltage level, the OVP pin reaches a 2.0V threshold. Once this threshold is reached, capacitor C9 from CTIMR to ground starts to charge with a 3uA current. When the CTIMR capacitor voltage reaches 3V, the IC immediately latches/shuts down. Using the approximation I = C ΔV/Δt, where I = 3uA, ΔV = 3V, we have the following approximate relationhip between the CTIMR capacitor and the time Δt before the IC shuts down:

$$C(uF) = \Delta t(s)$$

The time Δt should be set such that there will be enough time for the CCFL to ignite. If the CCFL ignites within this time, CTIMR will stop charging and the inverter will switch a normal operating frequency. Typically, for most lamps, ignition time is approximately 1 second.

Soft-Start Function

The OZ960 provides a soft-start function, which controls the gradual increase in overlap of the diagonal switches during start-up. During turn-on, this reduces inrush current and prevents unnecessary stresses both on the inverter components and the CCFL. The soft-start function is implemented by connecting a capacitor C12 from the SST pin to ground. The IC sources a current of 6uA to charge capacitor C12. For most applications, a value of 0.47uF is sufficient.

Open-Lamp Protection

In addition to overvoltage protection, the OZ960 provides protection when the lamp is suddenly removed or damaged during normal operation.

After the inverter is turned on and is in steady-state operation, the SST capacitor is fully charged to the +5V VDDA level. The CMP voltage is typically 2.3V at the nominal input voltage. If the lamp is suddenly removed or fails (opens), the IC will immediately shut down. This happens because the open-lamp protection circuitry is enabled when the SST level is above 4V (1V below VDDA) and is triggered when the CMP voltage goes above the 3.0V threshold. Since the current feedback is not sensed by R13, the CMP voltage level goes high and reaches a level beyond this threshold.

Control Loop Compensation

The control loop of a typical OZ960 inverter circuit can be easily compensated through adjustments of the compensation capacitor C16 between the FB and CMP pins. To improve the phase and gain margins, it is necessary to adjust the value of this capacitor, resulting in phase margins >45deg and gain margins >12dB.

PCB Layout Design Guidelines

As in most inverter designs, the performance of an OZ960 inverter can be highly influenced by the PCB layout. High-frequency switching currents, particularly in the ground traces, can greatly affect the stable operation and proper performance of the other inverter functions. These relatively high switching currents (MOSFET, transformer, gate drive and CCFL currents) disturb the low-level signals in the feedback and protection circuitry. As a result, it may cause the control function to act abnormal. To avoid these issues, a few recommended guidelines for PCB layout are listed below:

1. The most critical consideration regarding PCB layout is the grounding. It is very important to separate the power ground from the signal ground. The power ground consists of the input capacitor, transformer, power MOSFET, current sense resistor and OZ960 PGND grounds. The signal ground connects the ground points of the remaining components – OZ960 GNDA pin, Vcc capacitor ground, ground ends of the oscillator capacitors, resistors and other small-signal parts. The power ground and the signal ground must have separate traces on the PCB and their final connection point should be at the input connector ground terminal. A simplified OZ960 inverter schematic with a recommended grounding layout is shown in Figure 4, page 12. In the reference schematic, Figure 5, the power ground and signal ground are depicted with two different symbols and are connected together at the input connector ground.

2. Critical components such as RT, CT, and LCT resistors/capacitors and their associated copper traces must be kept away from high-current components/traces such as the MOSFETs, gate, drain and transformer traces. The ground pin of the LCT capacitor, Figure 4, must be directly connected to the ground pin of the Vcc capacitor to minimize ground noise effects during PWM operation.

3. The connection traces between the OZ960 drive outputs (NDR_B, PDR_A, PDR_C, NDR_D) and the MOSFET gates must be kept as short as possible. This minimizes EMI.

4. The connection traces between the MOSFET drains and the transformer primary winding must be kept as short as possible to minimize EMI and a lower power loss.

The design guidelines discussed in the preceding pages can be followed for any inverter design using the OZ960. For most designs, the typical values provide in this application note are sufficient. However, this is a guideline and further fine-tuning and adjustments may be required depending on the applications. Additional notes on the reference design follow.

RECOMMENDED GROUNDING LAYOUT FOR OZ960 INVERTER

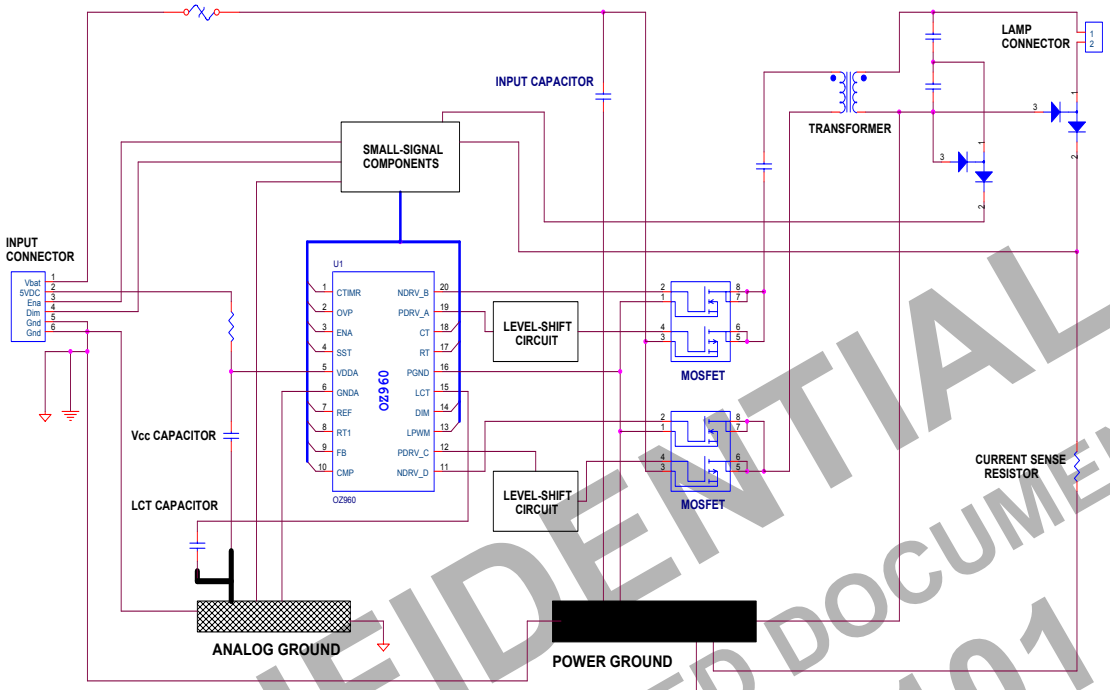


Figure 4

Notes on the Reference Design

1. This is an application design for a 14” CCFL panel with a typical current of 6.0mA.

2. The +5V power supply VDDA, to the OZ960, is derived from the main input voltage VIN through a linear series-pass regulator formed by Q2, D6, R14 and R16.

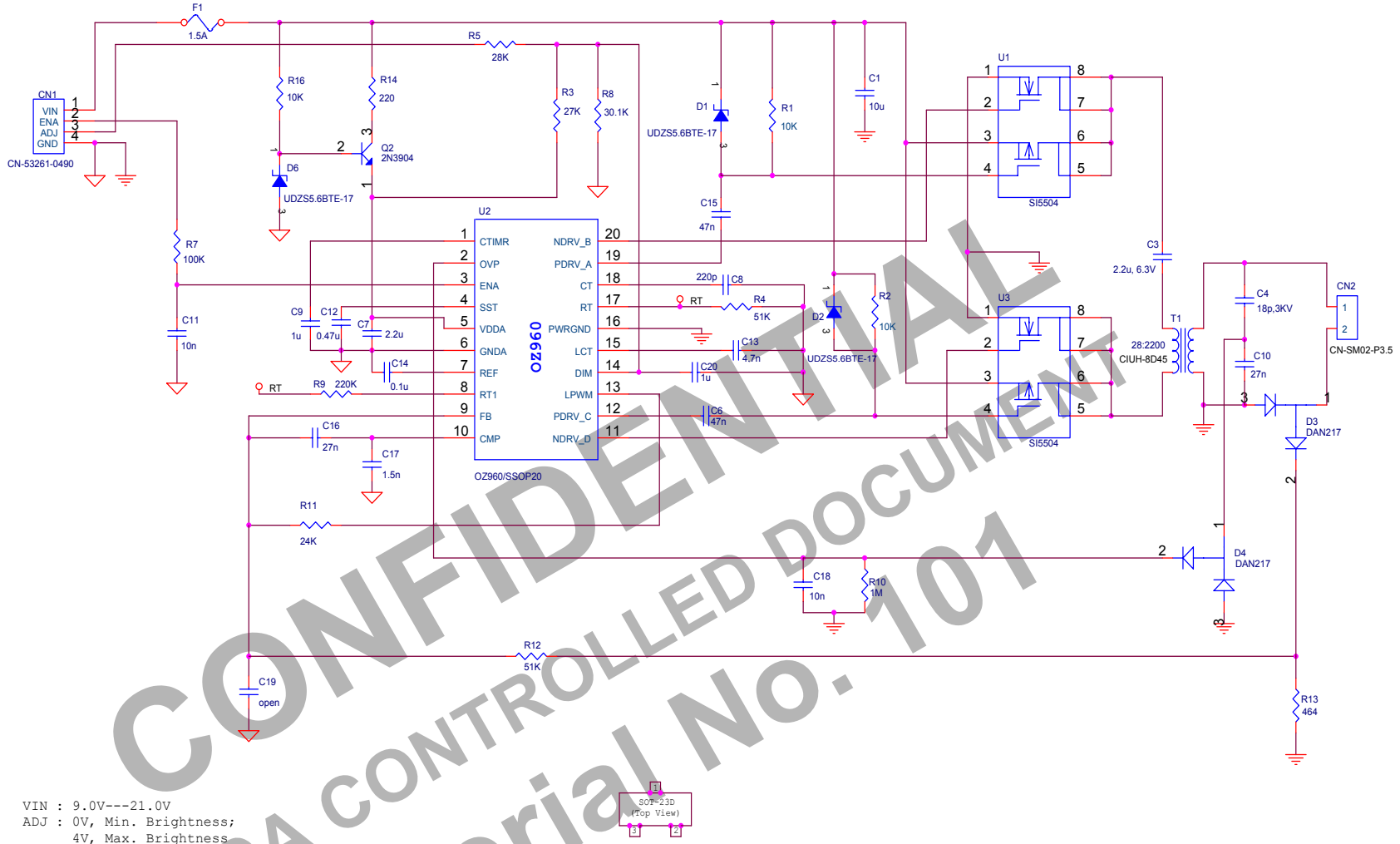
3. The external dimming control voltage ADJ has a range of 0-4V. The resistive network formed by R3, R5 and R8 provide a DIM voltage range of 1.7-3.0V which produces a lamp current range of 2.0-6.0mA.

4. The nominal operating frequency determined by R4 (51kΩ) and C8 (220pF) is ~61kHz.

5. The striking frequency determined by R4 (51kΩ) and R9 (220kΩ) in parallel and C8 (220pF) is ~78kHz.

6. The LPWM frequency determined by C13 (4.7nF) is ~318Hz.

OZ960 INVERTER REFERENCE DESIGN



VIN : 9.0V---21.0V
ADJ : 0V, Min. Brightness;
4V, Max. Brightness
ENA : Disable, 0 - 1V,
Enable, 2 - 5V

Figure 5

OZ960 INVERTER REFERENCE DESIGN
BILL OF MATERIALS

OZ960 INVERTER REFERENCE DESIGN Revised: Thursday, September 19, 2002
1.0 Revision: 00

Bill Of Materials September 19, 2002 15:50:11 Page1

Item	Qty	Reference	Part	PCB Footprint
1	1	CN1	CN-53261-0490	
2	1	CN2	CN-SM02-P3.5	
3	1	C1	10u 25V Y5V 20%	1210
4	2	C3, C7	2.2u 16V Y5V 20%	0805
5	1	C4	18p 3KV NPO 5%	1808
6	2	C15, C6	47n 25V X7R 10%	0603
7	1	C8	220p 50V NPO 5%	0603
8	2	C9, C20	1u 6.3V X5R 10%	0603
9	2	C10, C16	27n 25V X7R 10%	0603
10	2	C11, C18	10n 25V X7R 10%	0603
11	1	C12	0.47u 6.3V X5R 10%	0603
12	1	C13	4.7n 50V X7R 10%	0603
13	1	C14	0.1u 16V Y5V 20%	0603
14	1	C17	1.5n 50V Y5V 20%	0603
15	1	C19	open	0603
16	3	D1, D2, D6	5.6V	1206
17	2	D4, D3	DAN217	SOT-23D
18	1	F1	1.5A	1206
19	1	Q2	2N3904	SOT-23D
20	3	R1, R2, R16	10K	0603
21	1	R3	27K, 1%	0603
22	2	R12, R4	51K, 1%	0603
23	1	R5	28K, 1%	0603
24	1	R7	100K	0603
25	1	R8	30.1K, 1%	0603
26	1	R9	220K, 1%	0603
27	1	R10	1M	0603
28	1	R11	24K, 1%	0603
29	1	R13	464, 1%	0603
30	1	R14	220	0603
31	1	T1	28:2200	SUMIDA CIUH-8D45
32	2	U3, U1	SI5504	SO-8
33	1	U2	OZ960	SSOP-20