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MOTOROLA

MC44817/17B

PLL Tuning Circuits with 3-Wire Bus

The MC44817/17B are tuning circuits for TV and VCR tuner applications. They contain on one chip all the functions required for PLL control of a VCO. The integrated circuits also contain a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44817 has programmable 512/1024 reference divider while the MC44817B has a fixed reference divider of 1024.

The MC44817/17B are manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (3–Wire Bus). Data and Clock Inputs are IIC Bus Compatible
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider Accepts Input Frequencies up to 165 MHz
- Reference Divider: Programmable for Division Ratios 512 and 1024. The MC44817B has a Fixed 1024 Reference Divider
- Tri–State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Integrated PNP Band Buffers for 40 mA (V_{CC1} to 14.4 V)
- Output Options for the Reference Frequency and the Programmable Divider
- Bus Protocol for 18 or 19 Bit Transmission
- Extra Protocol for 34 Bit for Test and Further Features
- High Sensitivity Preamplifier
- Circuit to Detect Phase Lock
- Fully ESD Protected

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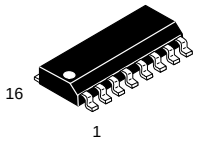
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44817D	T_A = –20° to +80°C	SO–16
MC44817BD		

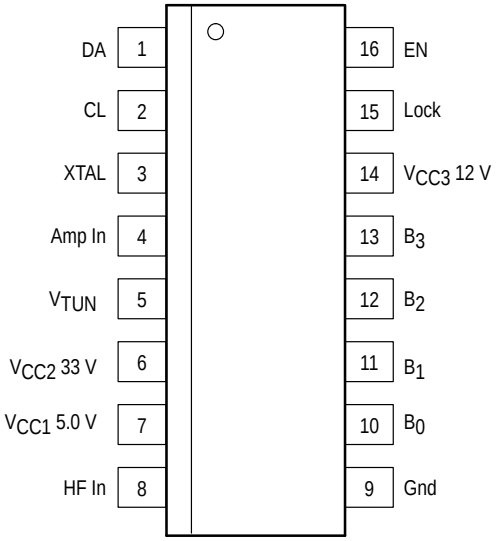
TV AND VCR PLL TUNING CIRCUITS WITH 1.3 GHz PRESCALER AND 3–WIRE BUS

SEMICONDUCTOR TECHNICAL DATA



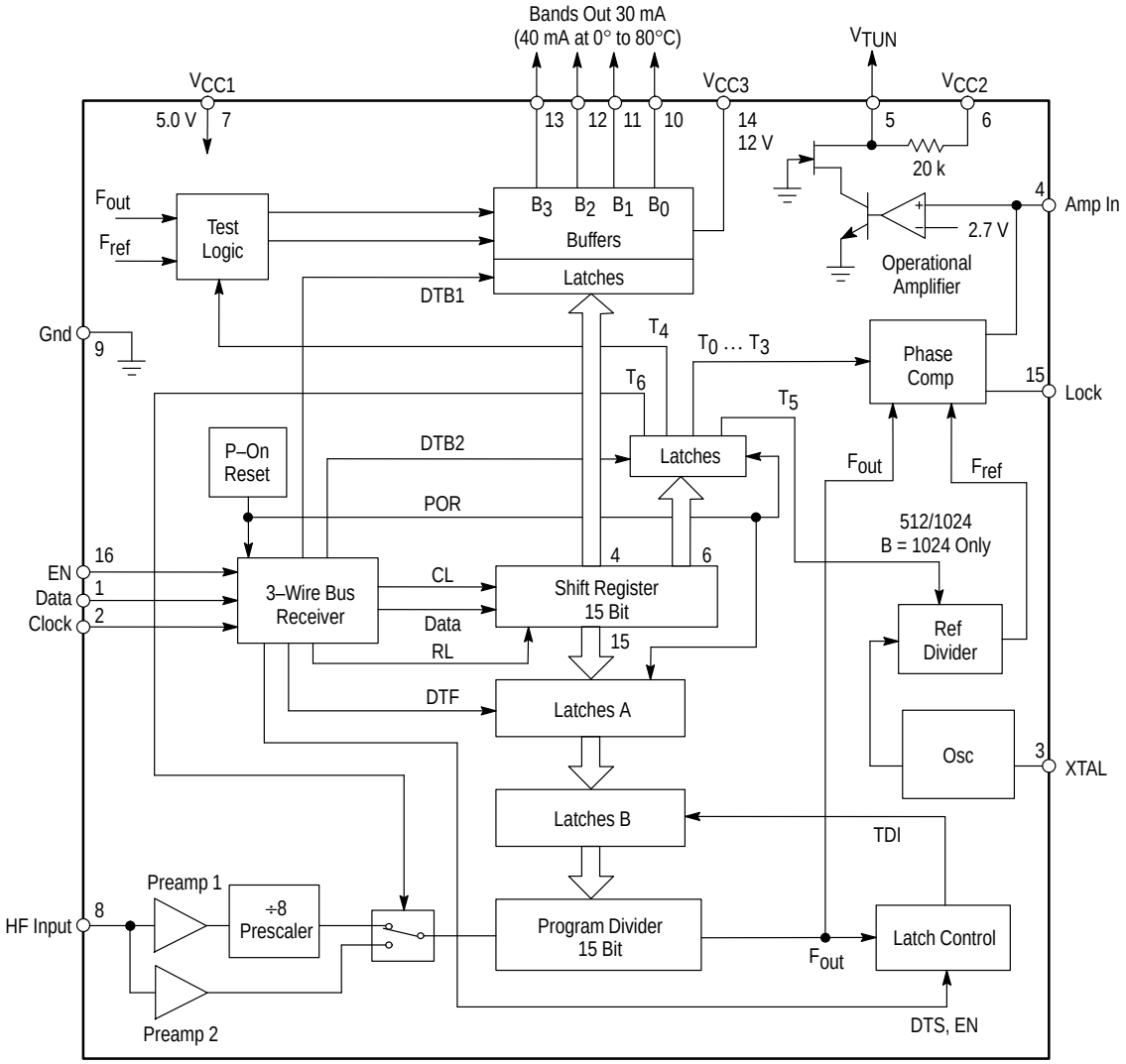
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS



(Top View)

Representative Block Diagram



This device contains 3,204 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin	Value	Unit
Power Supply Voltage (V_{CC1})	7	6.0	V
Band Buffer “Off” Voltage	10–13	14.4	V
Band Buffer “On” Current	10–13	50	mA
Band Buffer – Short Circuit Duration (0 to V_{CC3}) (Note 2)	10–13	Continuous	–
Operational Amplifier Power Supply Voltage (V_{CC2})	6	40	V
Operational Amplifier Short Circuit Duration (0 to V_{CC2})	5	Continuous	–
Power Supply Voltage (V_{CC3})	14	14.4	V
Storage Temperature	–	–65 to +150	°C
Operating Temperature Range	–	–20 to +80	°C
Band Buffer Operation (Note 1) at 50 mA each Buffer All Buffers “On” Simultaneously	10–13	10	sec
Operational Amplifier Output Voltage	5	V_{CC2}	V
RF Input Level (10 MHz to 1.3 GHz)	–	1.5	Vrms

NOTES: 1. At V_{CC3} = V_{CC1} to 14.4 V and T_A = –20° to +80°C.
2. At V_{CC3} = V_{CC1} to 14.4 V and T_A = –20° to +80°C one buffer “On” only.

ELECTRICAL CHARACTERISTICS (V_{CC1} = 5.0 V, V_{CC2} = 33 V, V_{CC3} = 12 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
V_{CC1} Supply Voltage Range	7	4.5	5.0	5.5	V
V_{CC1} Supply Current (V_{CC1} = 5.0 V)	7	–	37	50	mA
V_{CC2} Supply Voltage Range	6	25	–	37	V
V_{CC2} Supply Current (Output Open)	6	–	1.5	3.5	mA
Band Buffer Leakage Current when “Off” at 12 V	10–13	–	0.01	1.0	μA
Band Buffer Saturation Voltage when “On” at 30 mA	10–13	–	0.15	0.3	V
Band Buffer Saturation Voltage when “On” at 40 mA only for 0° to 80°C	10–13	–	0.2	0.5	V
Data/Clock/Enable Current at 0 V	1, 2, 16	–10	–	0	μA
Data/Clock/Enable Current at 5.0 V	1, 2, 16	0	–	1.0	μA
Data/Clock/Enable Input Voltage Low	1, 2, 16	–	–	1.5	V
Data/Clock/Enable Input Voltage High	1, 2, 16	3.0	–	–	V
Clock Frequency Range	2	–	–	100	kHz
Oscillator Frequency Range	3	3.15	3.2	4.05	MHz
Operational Amplifier Internal Reference Voltage	–	2.0	2.75	3.2	V
Operational Amplifier Input Current	4	–15	0	15	nA
DC Open Loop Voltage Gain	–	100	250	–	V/V
Gain Bandwidth Product (CL = 1.0 nF)	–	0.3	–	–	MHz
V_{out} Low, Sinking 50 μA	5	–	0.2	0.4	V
V_{out} High, Sourcing 10 μA, $V_{CC2} - V_{out}$	5	–	0.2	0.5	V
Phase Comparator Tri–State Current	4	–15	0	15	nA
Charge Pump High Current of Phase Comparator	4	30	50	85	μA
Charge Pump Low Current of Phase Comparator	4	10	15	30	μA
V_{CC3} Supply Voltage Range	14	V_{CC1}	–	14.4	V
V_{CC3} Supply Current	14				mA
All Buffers “Off”		–	0.2	0.5	
One Buffer “On” when Open		–	8.0	13	
One Buffer “On” at 40 mA		–	48	53	

Data Format and Bus Receiver

The circuit is controlled by a 3–wire bus via Data (DA), Clock (CL), and Enable (EN) inputs. The Data and Clock inputs may be shared with other inputs on the IIC–Bus while the Enable is a separate signal. The circuit is compatible with 18 and 19 bit data transmission and also has a mode for 34 bit transmission for test and additional features.

The 3–wire bus receiver receives data for the internal shift register after the positive going edge of the EN–signal. The data is transmitted to the band buffers on the negative going edge of the clock pulse 4 (signal DTB1).

18 and 19 Bit Data Transmission

The programmable divider may receive 14 bit (18 bit transmission) or 15 bit (19 bit transmission). The data is transmitted to the programmable divider (latches A) on the negative going edge of clock pulse 19 or on the negative edge of the EN–signal if EN goes down after the 18th clock pulse (signal DTF). If the programmable divider receives 14 bit, its MSB (bit N_{14}) is internally reset. The reset pulse is generated only if EN goes negative after the 18th clock pulse (signal RL).

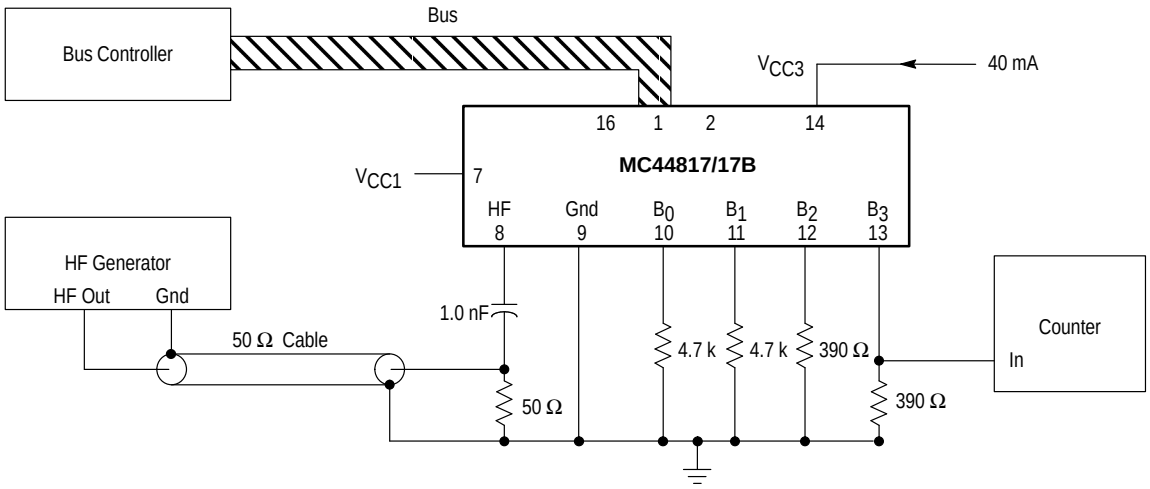
34 Bit Data Transmission
(For Test and Additional Features)

In the test mode, the programmable divider receives 15 bit and the data is transferred to latches A on the negative edge of clock pulse 19 (signal DTF). The information for test is received on clock pulses 20 to 26 and transmitted to the latches on the negative edge of pulse 34 (signal DTB2). These latches have a power–on reset. The power–on reset sets the programmable divider to a counting ratio of 256 or higher and resets the corresponding latches to the test bits T_0 to T_6 (signal POR). The bus receiver is not disturbed if the data format is wrong. Useless bits are ignored. If for example the Enable signal goes low after the clock pulse 9, bits one to four are accepted as valid buffer information and the other bits are ignored. If more than 34 bits are received, bit 35 and the following are ignored.

Lock Detector

The lock–detector output is low in lock. The output goes immediately high when an unlock condition is detected. The output goes low again when the loop is in lock during a complete period of the reference frequency.

Figure 1. HF Sensitivity Test Circuit



Device is in test mode. B_2, B_3 are "On" and B_0, B_1 are "Off".
Sensitivity is level of HF generator on 50 Ω load (without Pin 8 loading).

HF CHARACTERISTICS (See Figure 1)

Characteristic	Pin	Min	Typ	Max	Unit
DC Bias	8	–	1.6	–	V
Input Voltage Range					mVrms
10–80 MHz, Prescaler "Off", T_6 = 1.0	8	20	–	315	
80–150 MHz	8	10	–	315	
150–600 MHz	8	5.0	–	315	
600–950 MHz	8	10	–	315	
950–1300 MHz	8	50	–	315	

Figure 2. Typical HF Input Impedance

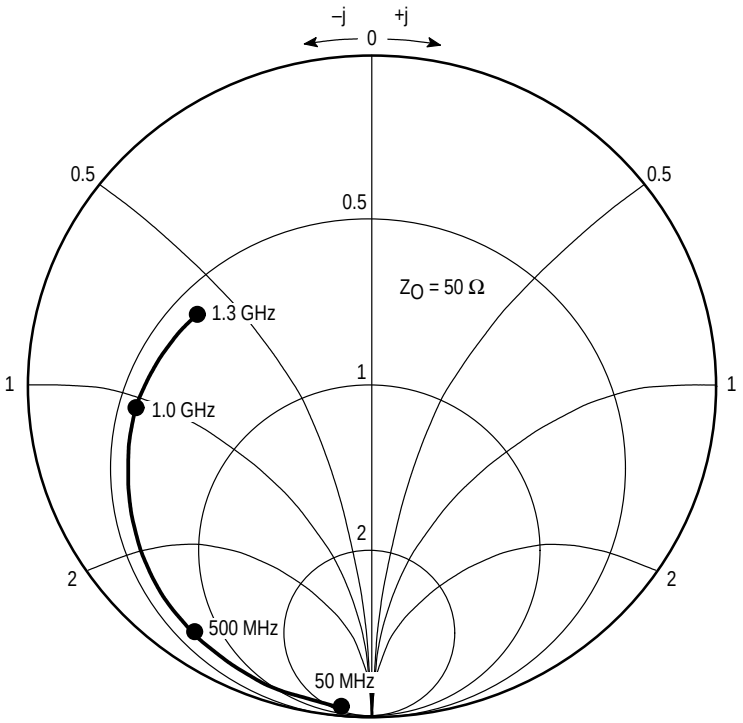
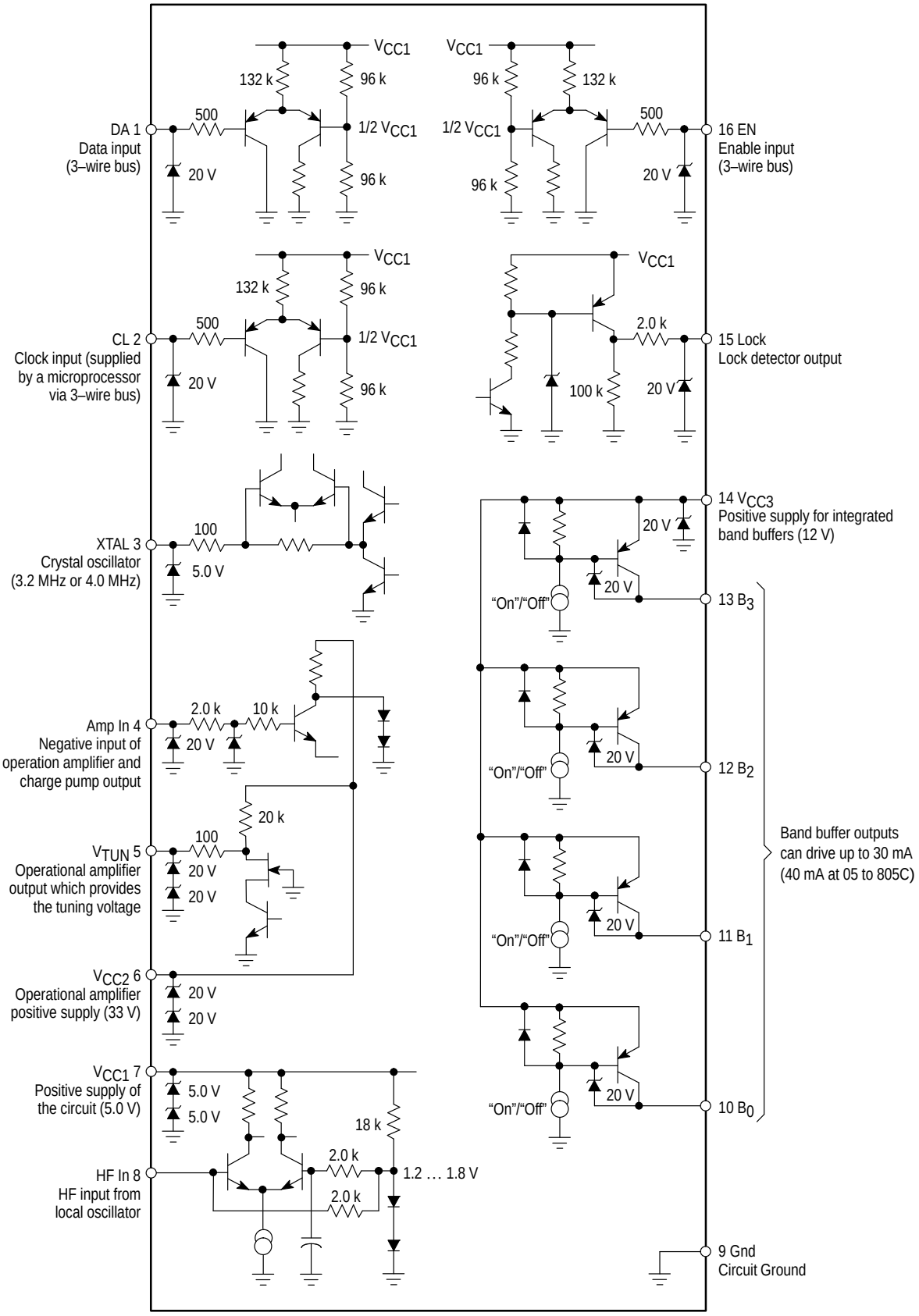
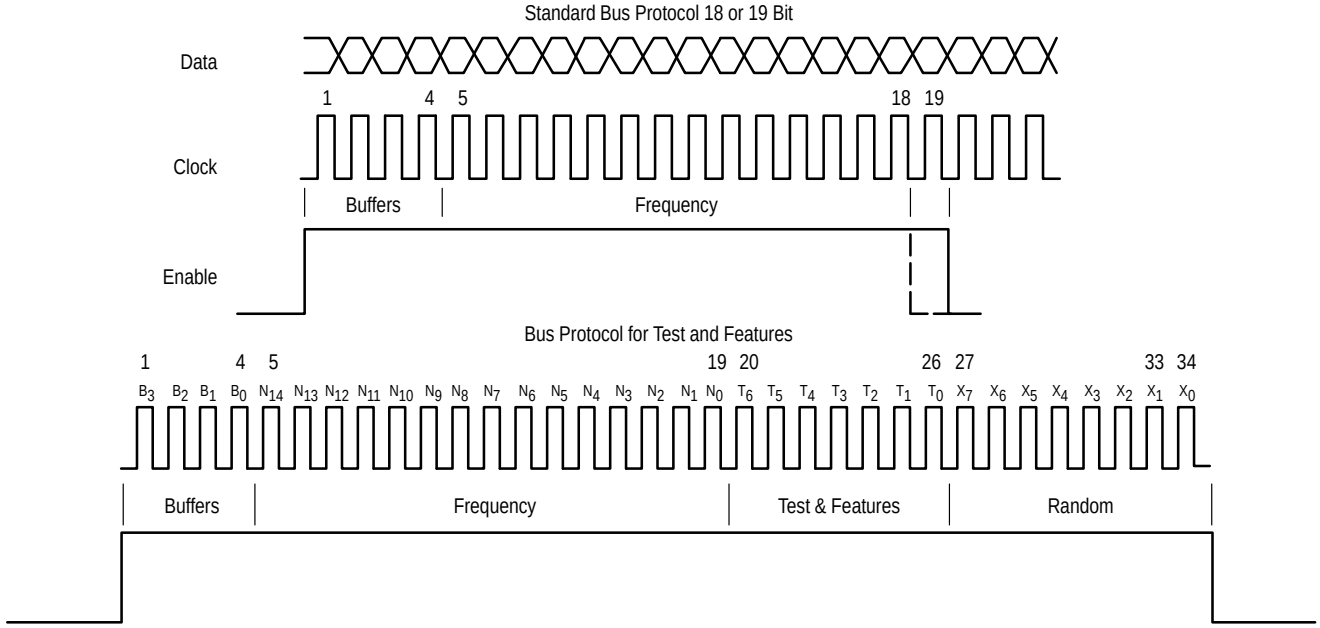


Figure 3. Pin Circuit Schematic



Bus Timing Diagram



Definition of Permissible Bus Protocols

1. Bus Protocol for 18 Bit
   B_3 B_2 B_1 B_0 N_{13} N_{12} N_{11} N_{10} N_9 N_8 N_7 N_6 N_5 N_4 N_3 N_2 N_1 N_0
   Max Counting Ratio 16363
   N_{14} is Reset Internally

2. Bus Protocol for 19 Bit
   B_3 B_2 B_1 B_0 N_{14} $N1_3$ N_{12} N_{11} N_{10} N_9 N_8 N_7 N_6 N_5 N_4 N_3 N_2 N_1 N_0
   Max Counting Ratio 32767
   – B_0 to B_3: Control of Band Buffers
   – N_0 to N_{14}: Control of Programmable Dividers

   N_{14} = MSB; N_0 = LSB
   Minimum Counting Ratio Always 17
   B_3 = First Shifted Bit
   N_0 = Last Shifted Bit

3. Bus Protocol for Test and Further Features (34 Bit)
   B_3 B_2 B_1 B_0 N_{14}…N_0 T_6 T_5 T_4 T_3 T_2 T_1 T_0 X_7 X_6…X_1 X_0
   – T_0 to T_3: Control the Phase Comparator
   – T_4: Switches Test Signals to the Buffer Outputs
   – T_5: Division Ratio of the Reference Divider
     B Version T_5 = “X”
   – T_6: Bypasses the Prescaler (Note 1)
   – X_0 to X_7: Are Random

   B_3 = First Shifted Bit
   X_0 = Last Shifted Bit

Definition of the Bits for Test and Features

Bit T_0: Defines the Charge Pump Current of the Phase Comparator

T_0 = 0	Pump Current 50 µA Typical
= 1	Pump Current 15 µA Typical

Bits T_1 and T_2: Define the Digital Function of the Phase Comparator

T_2	T_1	State	Output Function of Phase Comparator
0	0	1	Normal Operation
0	1	2	High Impedance (Tri–State)
1	0	3	Upper Source “On”, Lower Source “Off”
1	1	4	Lower Source “On”, Upper Source “Off”

NOTE: 1. The phase comparator pulls high if the input frequency is too high and it pulls low when the input frequency is too low. (Inversion by Operational Amplifier) The phase comparator generates a fixed duration offset pulse for each comparison pulse (similar to the MC44802A). This guarantees operation in the linear region. The offset pulse is a positive current pulse (upper source).

Bit T_3: Defines the Offset Pulse of the Phase Comparator

T_3 = 0	Offset Pulse Short (200 ns) Normal Mode
= 1	Offset Pulse Long (350 ns)

Bit T_4: Switches the Internal Frequencies F_{ref} and FBY2 to the Buffer Outputs (B_2, B_3)

T_4 = 0	Normal Operation
= 1	F_{ref} Switched to Buffer Output B_2 FBY2 Switched to Buffer Output B_3

NOTE: Bits B_2 and B_3 have to be one in this case.
F_{ref} is the reference frequency.
FBY2 is the output frequency of the programmable divider, divided by two.

Bit T_5: Defines the Division Ratio of the Reference Divider

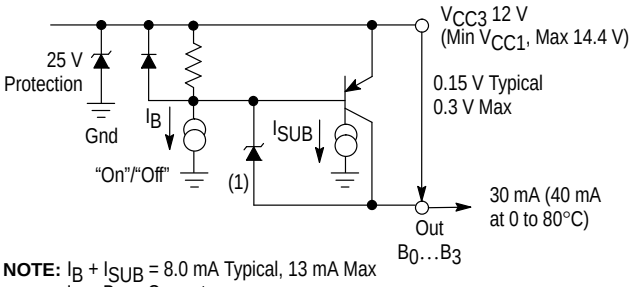
T_5 = 0	Division Ratio 512
= 1	Division Ratio 1024

NOTE: The division ratio of the reference divider can only be programmed in the 34 bit bus protocol.
In the standard bus protocol the division ratio is 512.
(The power–up reset POR sets the division ratio to 512).
On “B–version”, T_5 = “X”. Division ratio 1024 fixed.

Bit T_6: Switches the Prescaler

T_6 = 0	Normal Operation, 1.3 GHz
= 1	Low Frequency Operation Preamp. 2 Switched Off, 165 MHz maximum The prescaler is bypassed and the power supply of the prescaler is switched off. Input: 10 MHz minimum, 20 mVrms minimum

Figure 4. Equivalent Circuit of the Integrated Band Buffers



NOTE: $I_B + I_{SUB}$ = 8.0 mA Typical, 13 mA Max
I_B = Base Current
I_{SUB} = Substrate Current of PNP

The Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider; this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$N = 16384 \times N_{14} + 8132 \times N_{13} + \ldots + 4 \times N_2 + 2 \times N_1 + N_0$

Maximum Ratio 32767

(16363 in case of 18 bit bus protocol)

Minimum Ratio 17

$N_0 \ldots N_{14}$ are the different bits for frequency information.

At power–on the whole bus receiver is reset and the programmable divider is set to a counting ratio of N = 256 or higher.

The Prescaler

The prescaler has a preamplifier which guarantees high input sensitivity.

The Phase Comparator

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

The Operational Amplifier

The operational amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The operational amplifier needs 28.5 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28 V.

Figure 6 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

The Oscillator

The oscillator uses a 3.2 to 4.0 MHz crystal tied to ground in series with a capacitor. The crystal operates in the series resonance mode.

The voltage at Pin 3 has low amplitude and low harmonic distortion.

Figure 5. Equivalent Circuit of the Lock Output

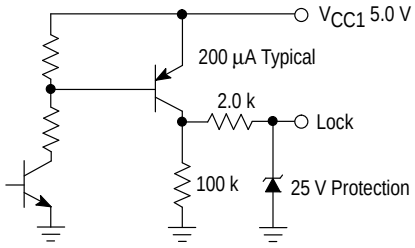
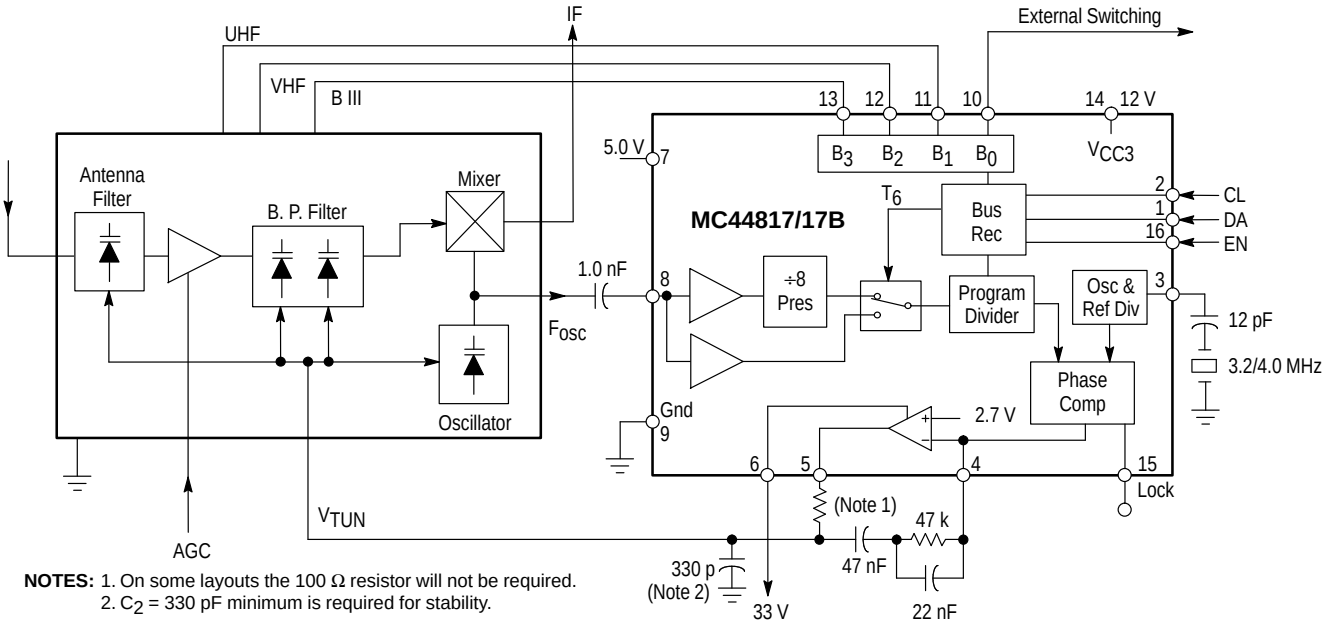


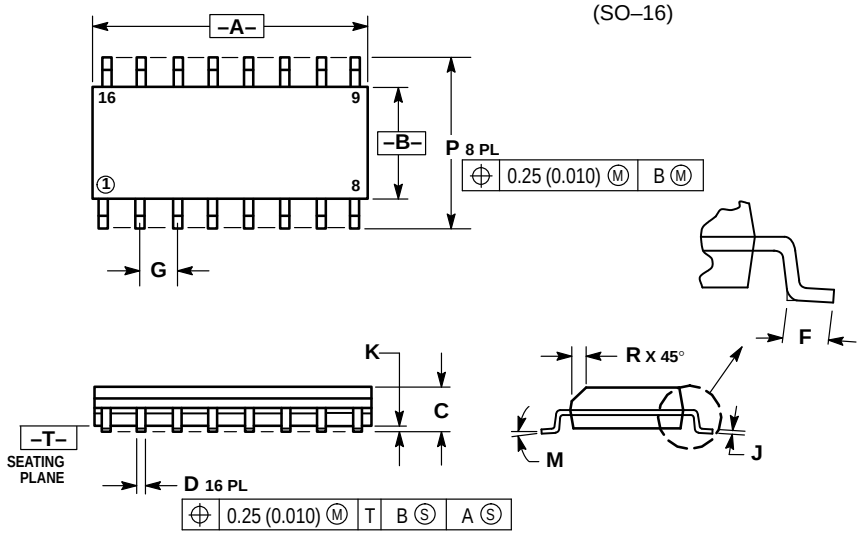
Figure 6. Typical Tuner Application



NOTES: 1. On some layouts the 100 Ω resistor will not be required.
2. C_2 = 330 pF minimum is required for stability.

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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