Ordering number : EN 4616

Monolithic Linear IC

SANYO No.4616

LA7945N

Closed Caption Signal (US specifications) Extraction IC

Overview

The LA7945N extracts the closed caption signal overlapped in the video signal vertical retrace period and transfers the data and clock signal to a decoder IC. This IC requires the use of either an add-on type decoder, such as the LC7458B or 7457A (for I^2C), or a microcontroller type decoder, such as the LC8640XX.

Functions

- Synchronization separation
- VCO
- Vertical countdown
- Horizontal countdown
- Data slicing
- Dual loop AFC
- Field discrimination
- Lock detection
- Vertical/horizontal pulse output

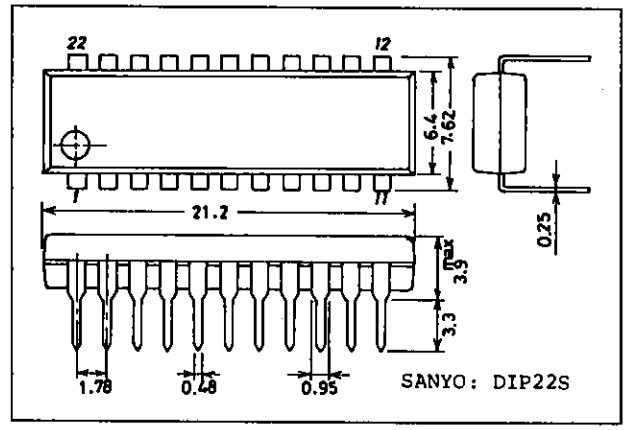
Features

- Adoption of a dual loop AFC allows the LA7945N to stably extract the caption signal.
- Provides the pulse outputs required by caption decoder ICs.

Package Dimensions

unit: mm

3059-DIP22S



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Condition	Rating	Unit
Maximum power supply voltage	V_{CC} max		7	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	250	mW
Operating temperature	Topr		−10 to +70	°C
Storage temperature	Tstg		−55 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Rating	Unit
Recommended power supply voltage	V_{CC}	5	V
Operating power supply voltage range	V_{CC} op	4.5 to 5.5	V

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Electrical and Operating Characteristics at Ta = 25°C, V_{CC} = 5.0 V, Input signal: sync-white 1.0 V

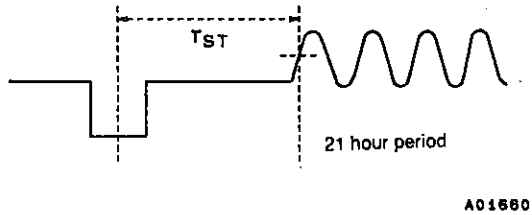
Parameter		Symbol	Rating			Unit
			min	typ	max	
Horizontal pull-in range		f_{HPULL}	±1.5			kHz
Horizontal free-running frequency		f_{HFREE}	15.3	15.7	16.3	kHz
Input clamping voltage		V_{CLMP}	2.3	2.5	2.7	V
H LOCK filter threshold level		V_{LOCKTH}	2.3	2.5	2.7	V
Synchronization separation output	High level	V_{SYNCH}	4.0	4.2	5.0	V
	Low level	V_{SYNCL}	0	0.8	1.0	V
H LOCK filter	High level	V_{LOCKH}	4.0	4.2	5.0	V
	Low level	V_{LOCKL}	0	0.8	1.0	V
Data output	High level	V_{DATAH}	4.0	4.2	5.0	V
	Low level	V_{DATAL}	0	0.8	1.0	V
Clock output	High level	V_{CLKH}	4.0	4.2	5.0	V
	Low level	V_{CLKL}	0	0.8	1.0	V
21H output	High level	V_{21HH}	4.0	4.2	5.0	V
	Low level	V_{21HL}	0	0.8	1.0	V
	Pulse width	V_{21HW}	60	65	70	µs
O/E output	High level	V_{OEH}	4.0	4.2	5.0	V
	Low level	V_{OEL}	0	0.8	1.0	V
	Pulse width	V_{OEW}	16.4	16.7	17.0	ms
Horizontal pulse output	High level	V_{HSH}	4.0	4.2	5.0	V
	Low level	V_{HSL}	0	0.8	1.0	V
	Pulse width	V_{HSW}	7.4	7.7	8.0	µs
Vertical pulse output	High level	V_{RSTH}	4.0	4.2	5.0	V
	Low level	V_{RSTL}	0	0.8	1.0	V
	Pulse width	V_{RSTW}	30.8	31.8	32.8	µs
Input signal level		VIN	−6	0	+3	dB
CLK-RUN-IN start time		TST	6.6	7.6	8.6	µs
Current dissipation		ICC	14.0	18.0	22.0	mA

Note: Must not be pulled in to any frequency other than f_H.
The pin 11 capacitor should be 100 pF ±5%.
The pin 12 resistor should be 15 kΩ ±1%.

Test Conditions

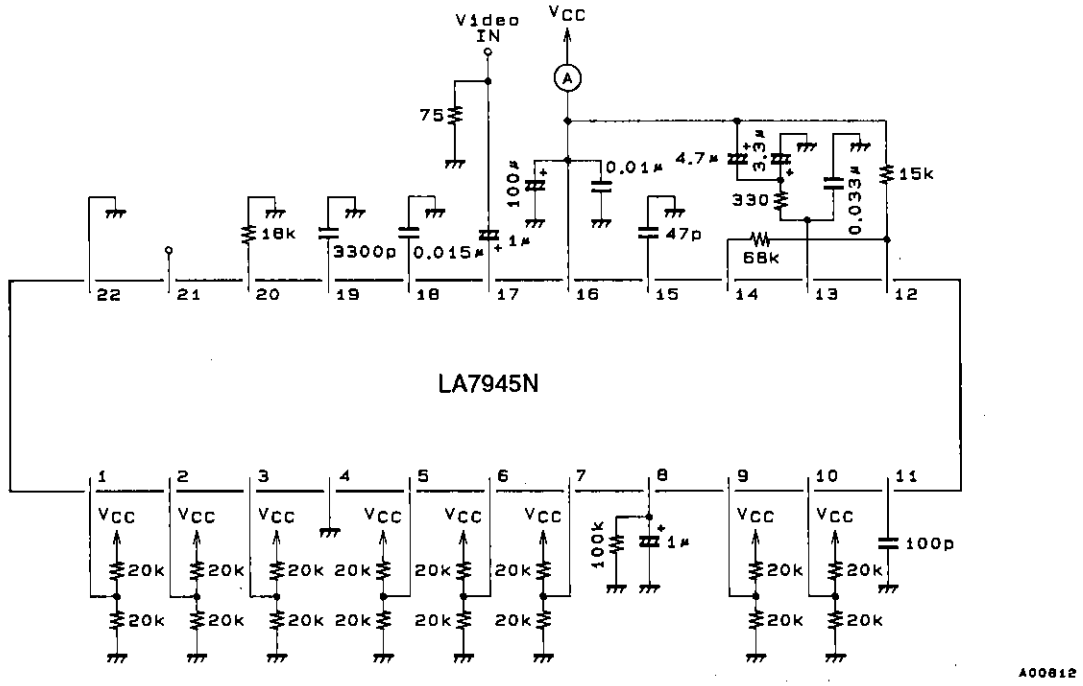
Parameter		Symbol	Test point	Test method
Horizontal pull-in range		f_{HPULL}	Pins 2 and 10	Vary the frequency f_H of the input signal and measure the point where the phase of pins 2 and 10 locks using an oscilloscope.
Horizontal free-running frequency		f_{HFREE}	Pin 10	Use a frequency counter to measure the frequency when there is no signal.
Input clamping voltage		V_{CLMP}	Pin 17	Measure the pedestal level with an oscilloscope.
H LOCK filter threshold level		V_{LOCKTH}	Pin 7	Measure the voltage at which pin 7 goes high by applying a DC voltage to pin 8 and varying that voltage.
Synchronization separation output	High level	V_{SYNCH}	Pin 2*1	Measure the pin 2 high and low levels with an oscilloscope.
	Low level	V_{SYNCL}		
H LOCK filter	High level	V_{LOCKH}	Pin 7*1	Measure the pin 7 high and low levels with an oscilloscope.
	Low level	V_{LOCKL}		
Data output	High level	V_{DATAH}	Pin 3*1, 2	Measure the pin 3 high and low levels with an oscilloscope.
	Low level	V_{DATAL}		
Clock output	High level	V_{CLKH}	Pin 5*1, 2	Measure the pin 5 high and low levels with an oscilloscope.
	Low level	V_{CLKL}		
21H output	High level	V_{21HH}	Pin 1*1	Measure the pin 1 high and low levels and the length of the high level period with an oscilloscope.
	Low level	V_{21HL}		
	Pulse width	V_{21HW}		
O/E output	High level	V_{OEH}	Pin 6*1	Measure the pin 6 high and low levels and the length of the high level period with an oscilloscope.
	Low level	V_{OEL}		
	Pulse width	V_{OEW}		
Horizontal pulse output	High level	V_{HEH}	Pin 10*1	Measure the pin 10 high and low levels and the length of the high level period with an oscilloscope.
	Low level	V_{HSL}		
	Pulse width	V_{HSW}		
Vertical pulse output	High level	V_{RSTH}	Pin 9*1	Measure the pin 9 high and low levels and the length of the high level period with an oscilloscope.
	Low level	V_{RSTL}		
	Pulse width	V_{RSTW}		
Input signal level		VIN	Each of pins 1, 3, 5, and 6*2	Vary the signal level input to pin 17, and confirm that the pin 1, 3, 5, and 6 outputs are operating correctly.
CLK-RUN-IN start time		TST	Each of pins 1, 3, 5, and 6*2, 3	Vary the time between SYNC and CLK-RUN-IN, and confirm that the pin 1, 3, 5, and 6 outputs are operating correctly.
Current dissipation		ICC	Pin 16*2	Connect a current meter to pin 16, and measure the current during decoding.

Notes: 1. Connect a 20 kΩ resistor between the pin being measured and V_{CC}, and also connect a 20 kΩ from that measurement pin to GND.
2. During measurement, this pin carries the closed caption encoded signal.
3. Time TST is shown in the figure below.



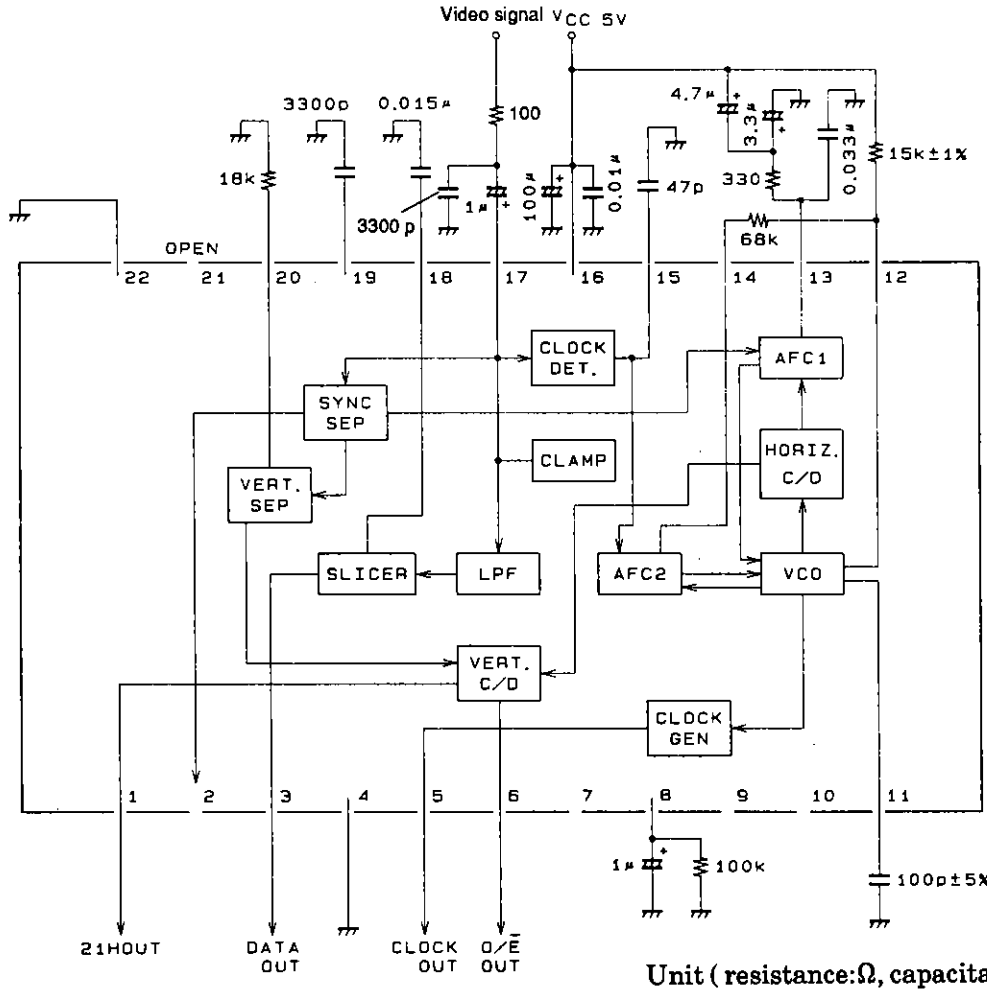
A01660

Test Circuit Diagram



Unit (resistance:Ω, capacitance:F)

Application Circuit Diagram



Unit (resistance:Ω, capacitance:F)

Pin Descriptions

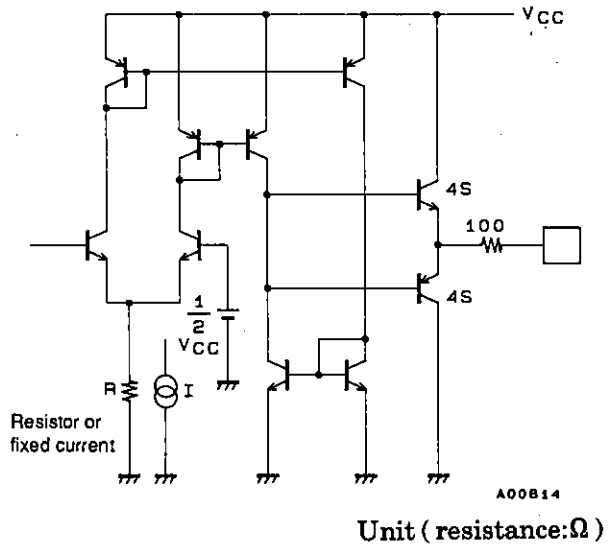


Figure 1

- The peripheral circuit for the pins described below is shown in figure 1. Either a resistor or a fixed current supply is connected to the lower side (the side away from the pin) of the differential amplifier.

Pin 1 (21H OUT): R = 18 kΩ. This signal goes high during the 21H and 284H periods. The fall of this signal is taken as the completion of data transfer.

Pin 2 (sync SEP): R = 9 kΩ. Synchronization separation output, see pin 19.

Pin 3 (DATA OUT): I ≈ 280 μA. Outputs the data overlapped with the vertical retrace period.

Pin 5 (CLOCK OUT): R = 9 kΩ. A clock output whose phase matches that of DATA OUT.

Pin 6 (O/$\overline{E}$ OUT): R = 18 kΩ. Field discrimination signal. High on odd fields.

Pin 7 (H LOCK OUT): I ≈ 50 μA. A resistor and capacitor are connected to pin 8, and this pin goes high when the internal VCO and the input signal are synchronized.

Pin 9 (V PULSE OUT): R = 18 kΩ. Set low during the 0.5H period synchronized with the vertical synchronization signal.

Pin 10 (H PULSE OUT): R = 18 kΩ. Outputs a low signal synchronized with the horizontal synchronization signal.

- Pin 8 (H LOCK FILTER): The H LOCK detection filter is connected to this pin.

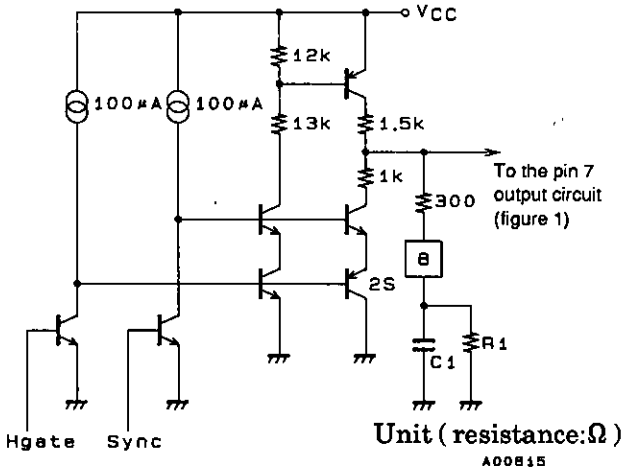


Figure 2: Pin 8 (H LOCK FILTER) Peripheral Circuit

Pin 8 is charged when the H gate and Sync phases match, and this voltage is compared and output to pin 7. The resistor R1 is used for discharge. The time from internal VCO locking until pin 7 goes high, and the time from lock release to the pin going low can be adjusted by changing the values of C1 and R1. If the pin 7 H LOCK OUT output is not used, C1 and R1 will be unnecessary.

- Pin 11 (VCO C): The capacitor for the $32f_H$ VCO is connected to this pin. (Error: 5%)

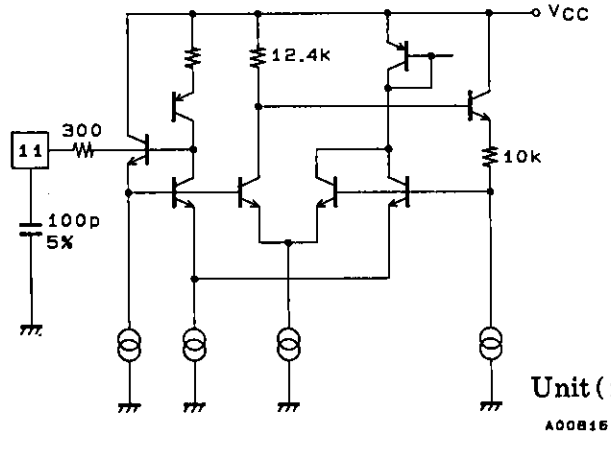


Figure 3: Pin 11 (VCO C) Peripheral Circuit

The LA7945N generates the $32f_H$ oscillation not by using a ceramic resonator, but by charging this capacitor with the fixed current defined by the resistance connected at pin 12. The horizontal pulses and the clock output from pin 5 are generated using this oscillator as a reference.

• Pin 12 (VCO R): The resistor for the $32f_H$ VCO is connected to this pin. (Error: 1%)

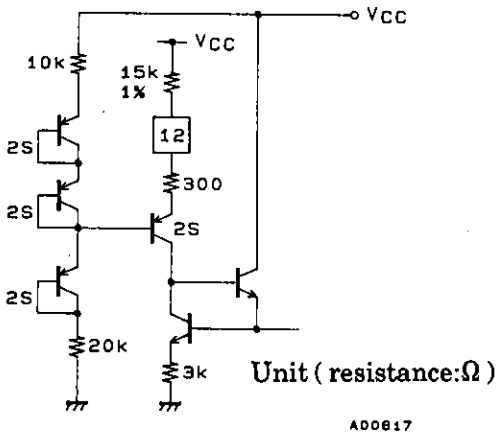


Figure 4: Pin 12 (VCO R) Peripheral Circuit

This resistor defines the current that charges the pin 11 capacitor. A DC voltage of 2/3 that of V_{CC} is output from pin 12.

• Pin 13 (AFC1): The horizontal AFC filter is connected to this pin.

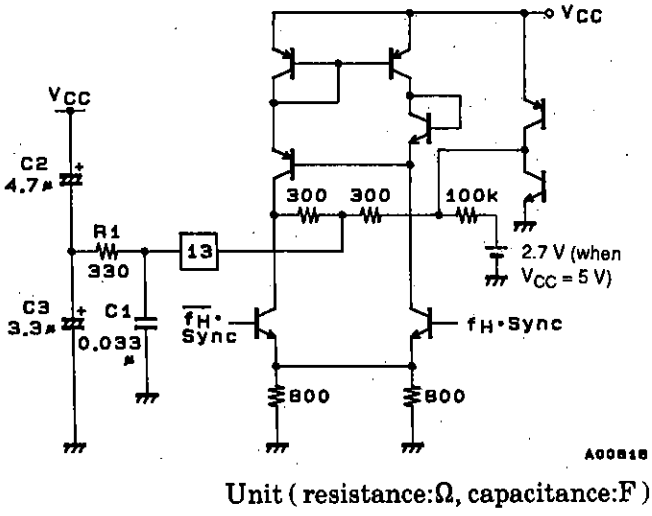
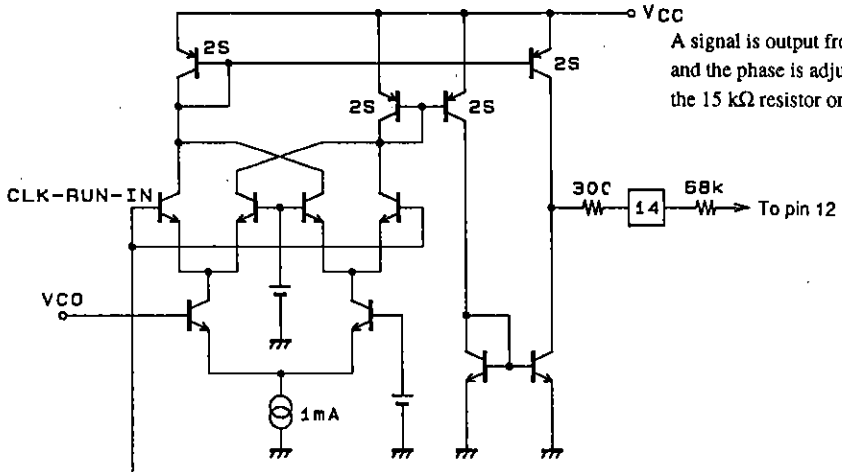


Figure 5: Pin 13 (AFC1) Peripheral Circuit

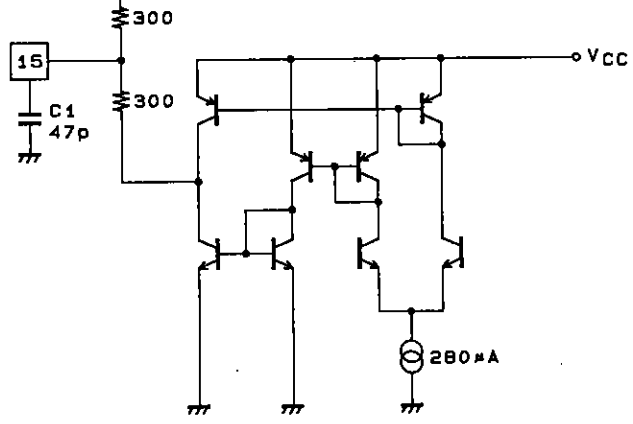
Although the ability to follow horizontal fluctuations improves as R1 increases, the holding power is reduced. Select this value according to the application circuit. Since the closed caption signal is overlapped with 21H, the VCO in this IC is influenced by signals such as the vertical synchronization signal and the copy guard signal. The values of C2 and C3 should be determined so that the VCO is stable with respect to these signals. To stabilize pin 13 at a voltage of about 2.7 V (when V_{CC} = 5 V) with no input, the ratio of C2 and C3 should be set so that this voltage takes on a value close to that of pin 13 when power is first applied.

• Pin 14 (AFC2): Used for phase adjustment of the internal VCO CLOCK and CLK-RUN-IN.



A signal is output from pin 14 only during the 21H CLK-RUN-IN period, and the phase is adjusted by controlling the fixed current determined by the 15 kΩ resistor on pin 12 only during that period.

• Pin 15 (CLOCK PHASE): CLOCK-RUN-IN phase compensation pin.

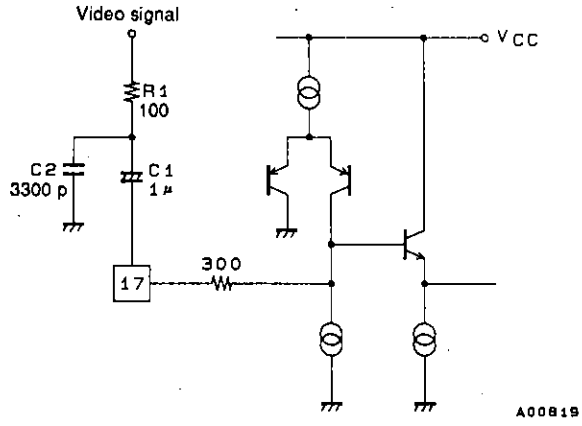


Only the CLK-RUN-IN signal during the vertical retrace period is extracted and passed to the multiplier described above. The phase of the clock output from pin 5 can be adjusted by the value of the capacitor (C1) connected to this pin.

Unit (resistance:Ω, capacitance:F) A00870

Figure 6: Pin 14 (AFC2) and Pin 15 (CLOCK PHASE) Peripheral Circuits

• Pin 17 (VIDEO IN): The video input pin. (sync-white 1 Vp-p)

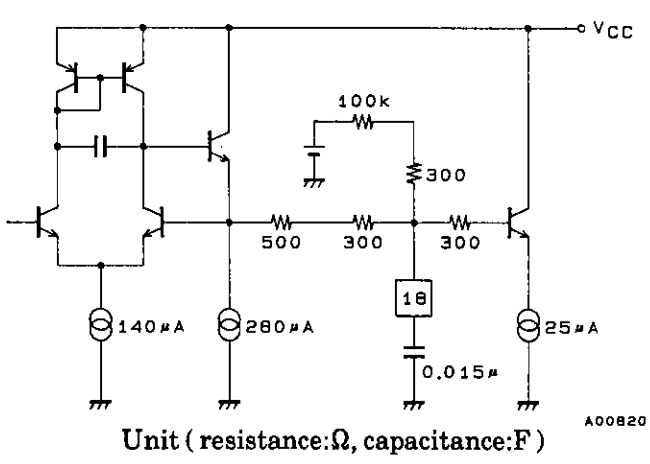


Pin 17 is designed to clamp the pedestal level at 1/2 V_{CC}. Since C1 also functions as the clamping capacitor, it should be driven with a low impedance (less than 500 Ω). The low field performance can be improved by adding an LPF such as R1 and C2. If this LPF is used, R1 must be a low resistance that can meet the conditions described above.

Unit (resistance:Ω, capacitance:F)

Figure 7: Pin 17 (VIDEO IN) Peripheral Circuit

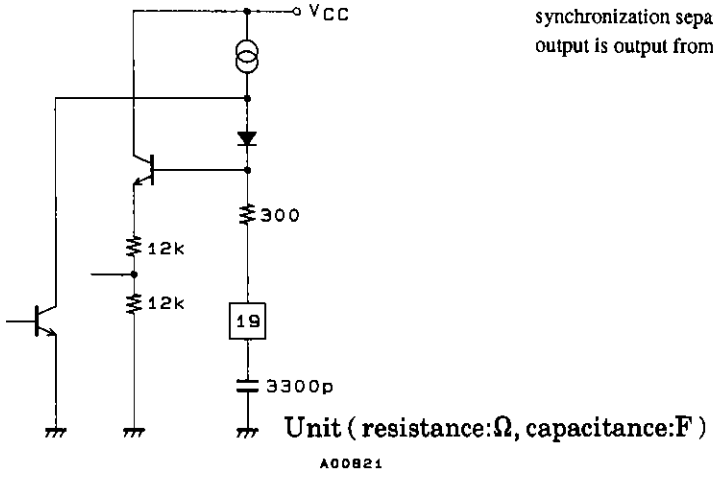
- Pin 18 (DATA LPF): The data slice LPF is connected to this pin.



A signal is output from pin 18 during the vertical retrace period CLK-RUN-IN period, and an LPF, which is used to detect the average value of CLK-RUN-IN (to be used as the slice level), is connected to this pin.

Figure 8: Pin 18 (DATA LPF) Peripheral Circuit

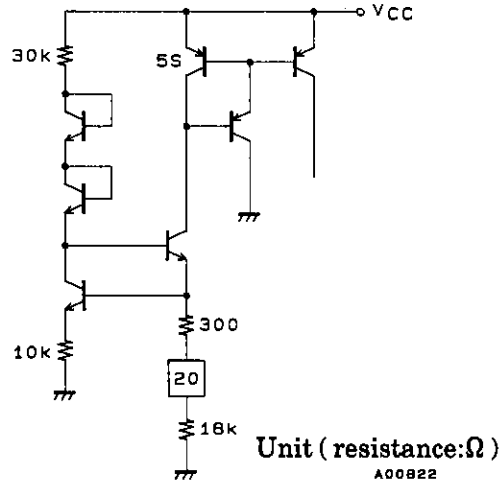
- Pin 19 (PEAK HOLD): The synchronization separator peak hold capacitor is connected to this pin.



This IC holds the peak value of sync on pin 19, and performs synchronization separation using 1/2 this level as the reference. This output is output from pin 2.

Figure 9: Pin 19 (PEAK HOLD) Peripheral Circuit

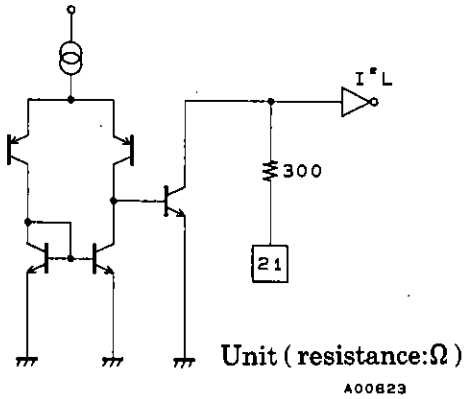
- Pin 20 (V SEP R): The resistor that determines the vertical synchronization separation is connected to this pin.



The LA7945N performs vertical synchronization separation by charging an internal capacitor using the fixed current determined by the resistor connected to this pin as the reference. The pin 20 DC voltage is 1/4 V_{CC}.

Figure 10: Pin 20 (V SEP R) Peripheral Circuit

• Pin 21: The vertical synchronization separation output pin.



The signal passed to the vertical C/D from vertical synchronization separation is output from pin 21. Since vertical C/D is I^2L, a signal of between 0 and 0.7 V is output. This pin is normally left open. The vertical C/D start position can be changed by an external override input.

Figure 11: Pin 21 Peripheral Circuit

• Pin 22: This pin determines whether or not the horizontal count for vertical C/D is changed every frame when the start bit is not detected.

When this pin is grounded, 21H is fixed, and it functions when open. Ground this pin when captions are used.

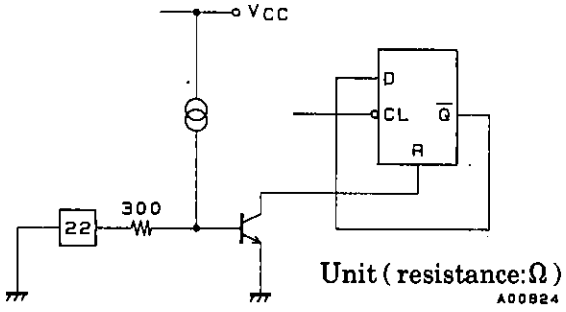


Figure 12: Pin 22 Peripheral Circuit

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